

Figure 1
PRIOR ART

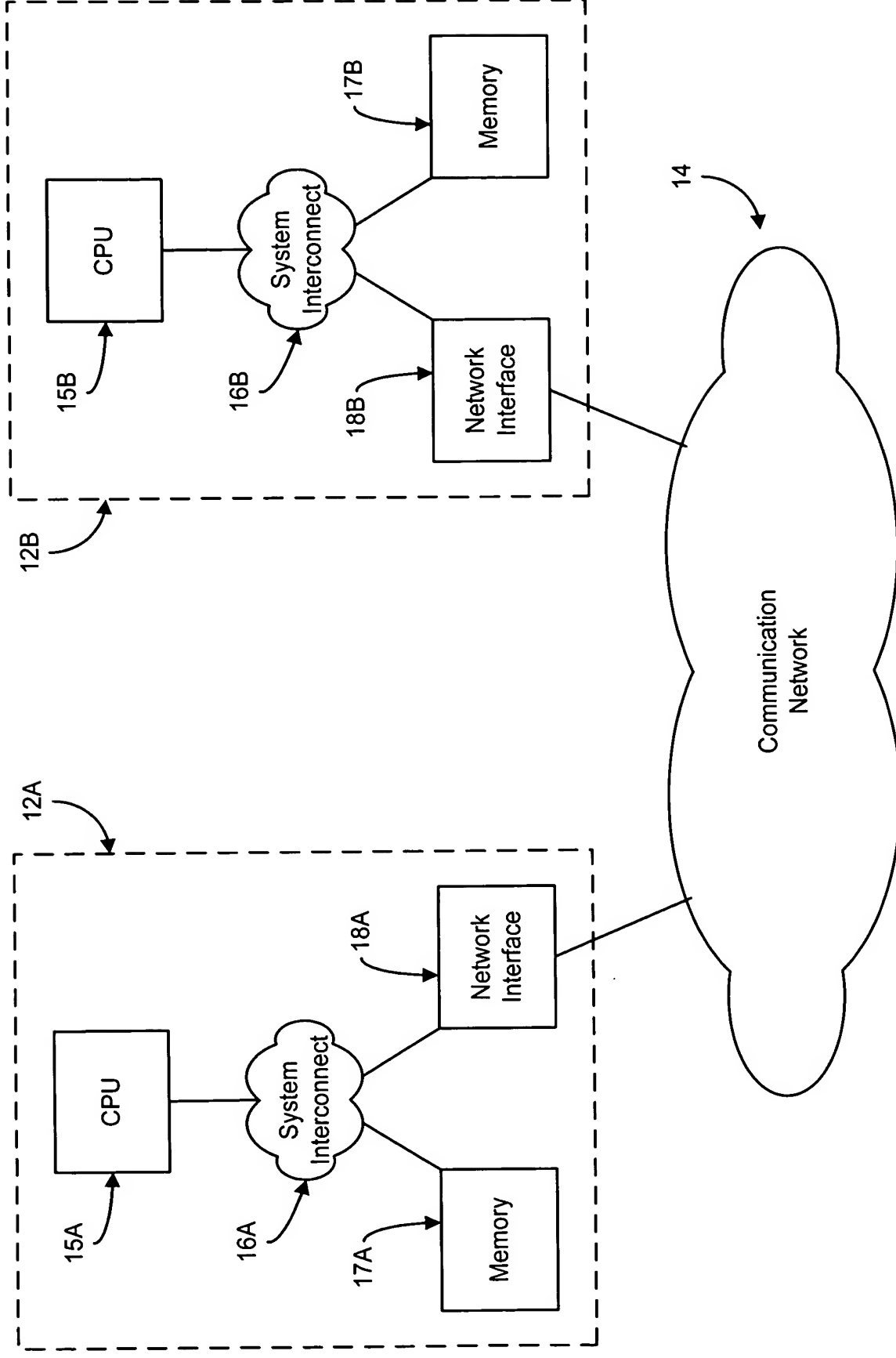


Figure 2
PRIOR ART

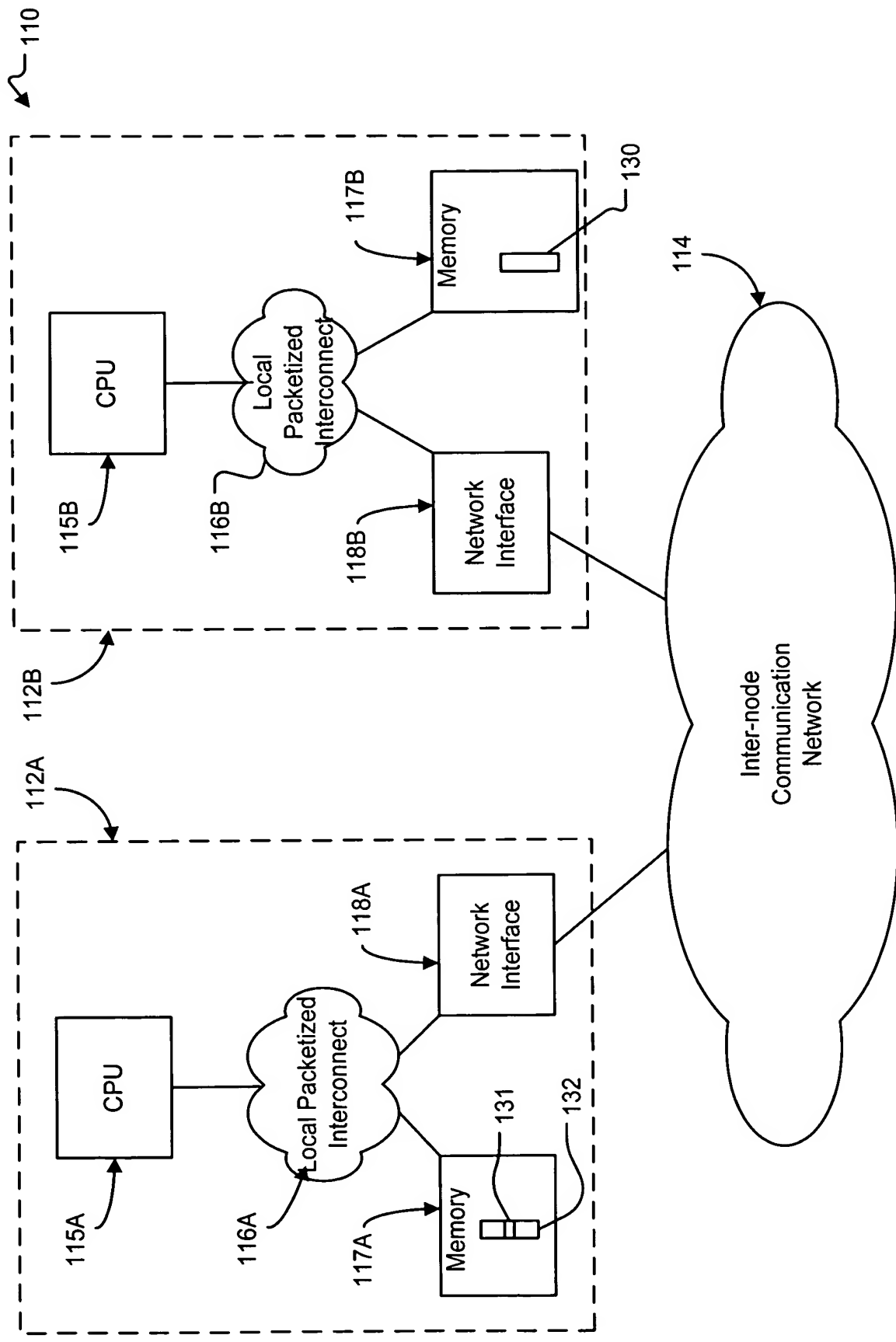


Figure 2A

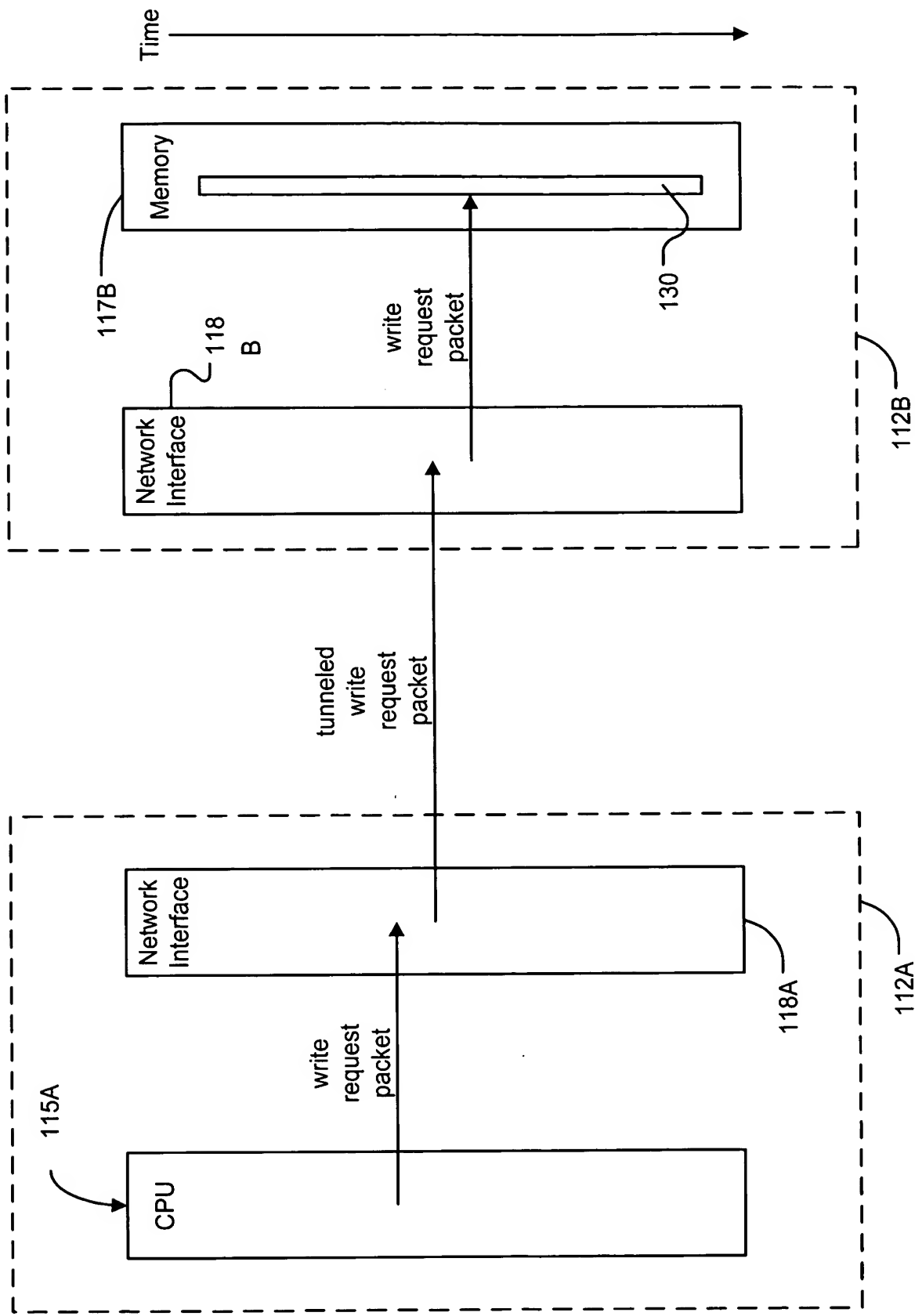


Figure 3

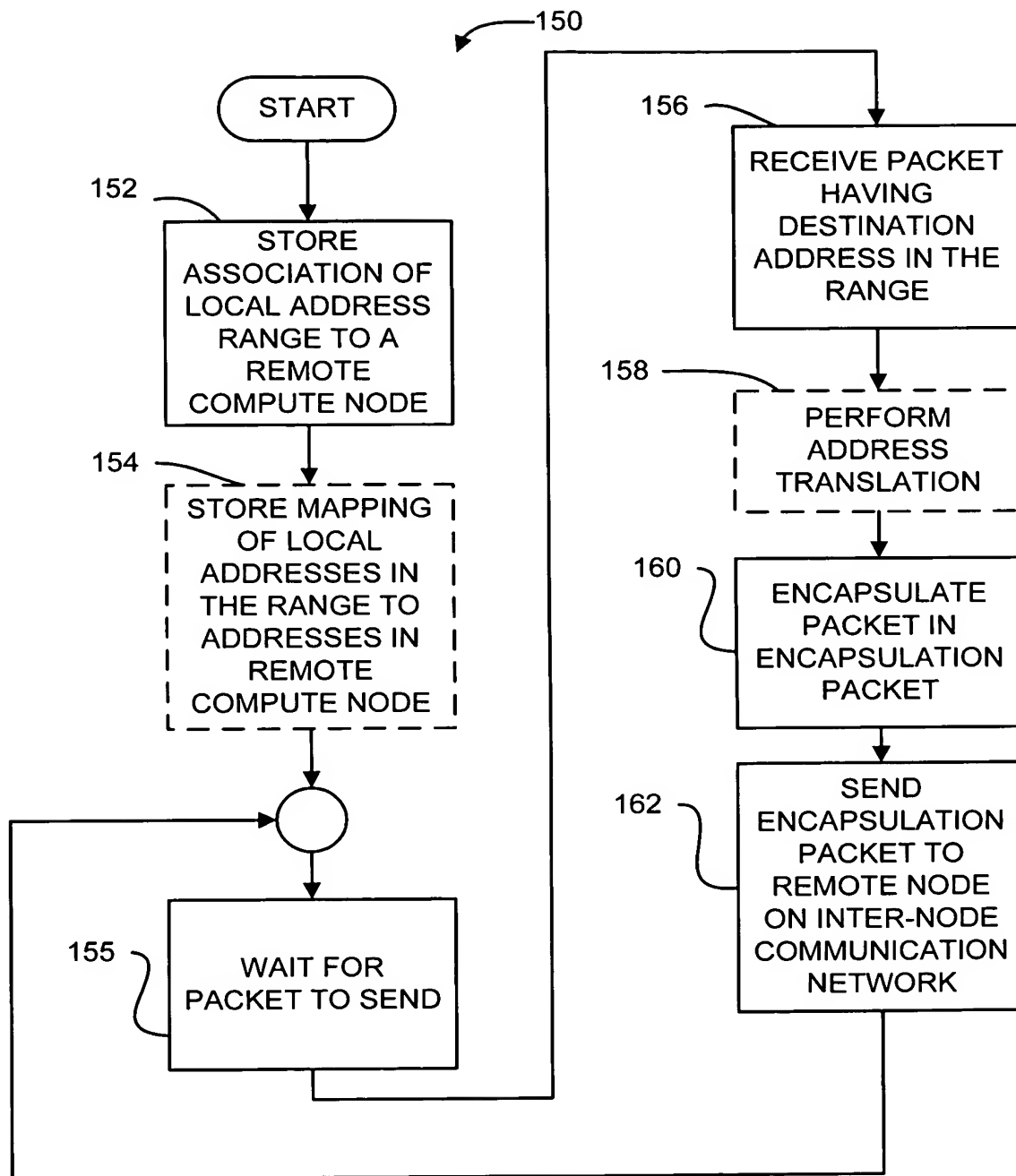


Figure 3A

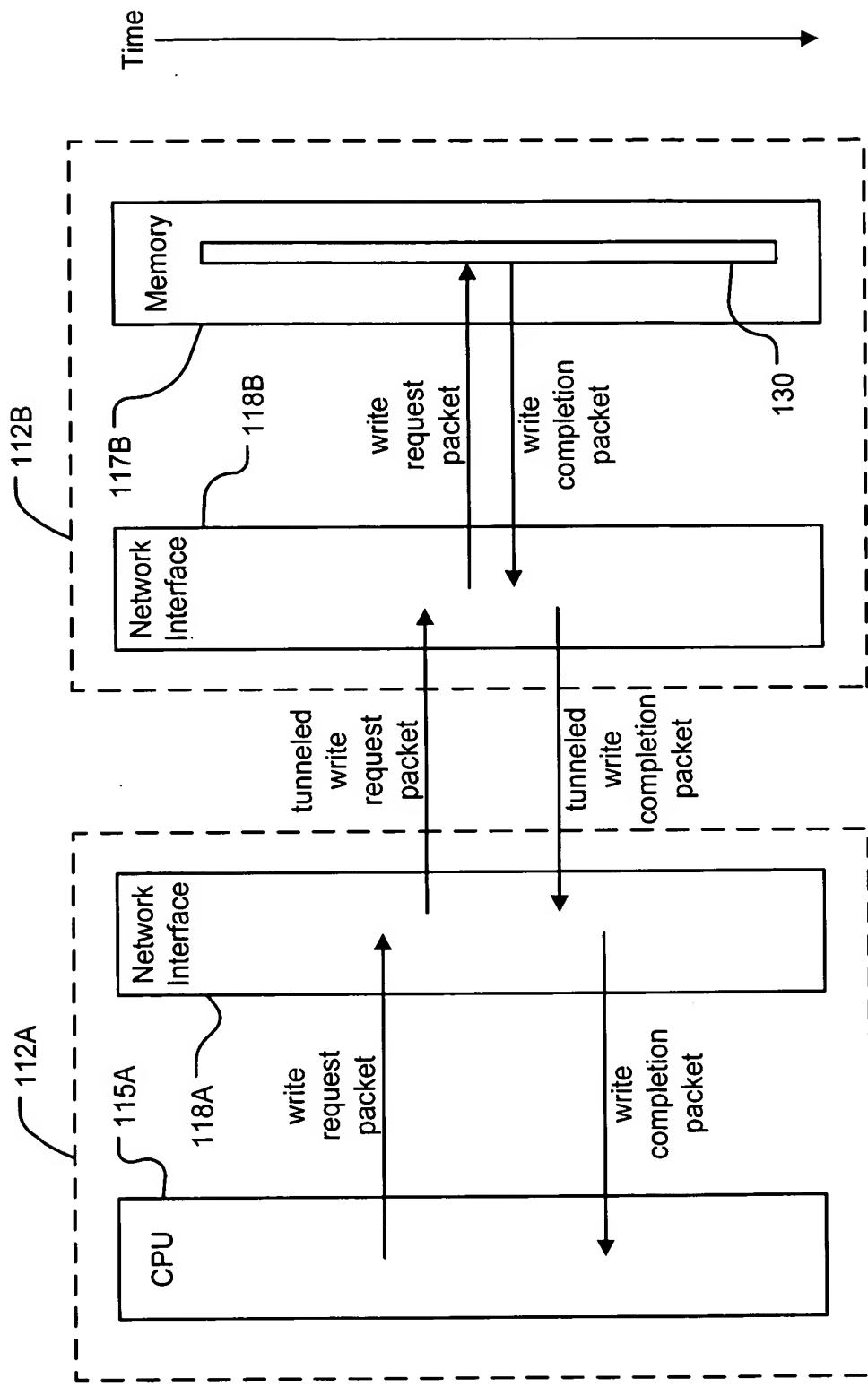


Figure 4

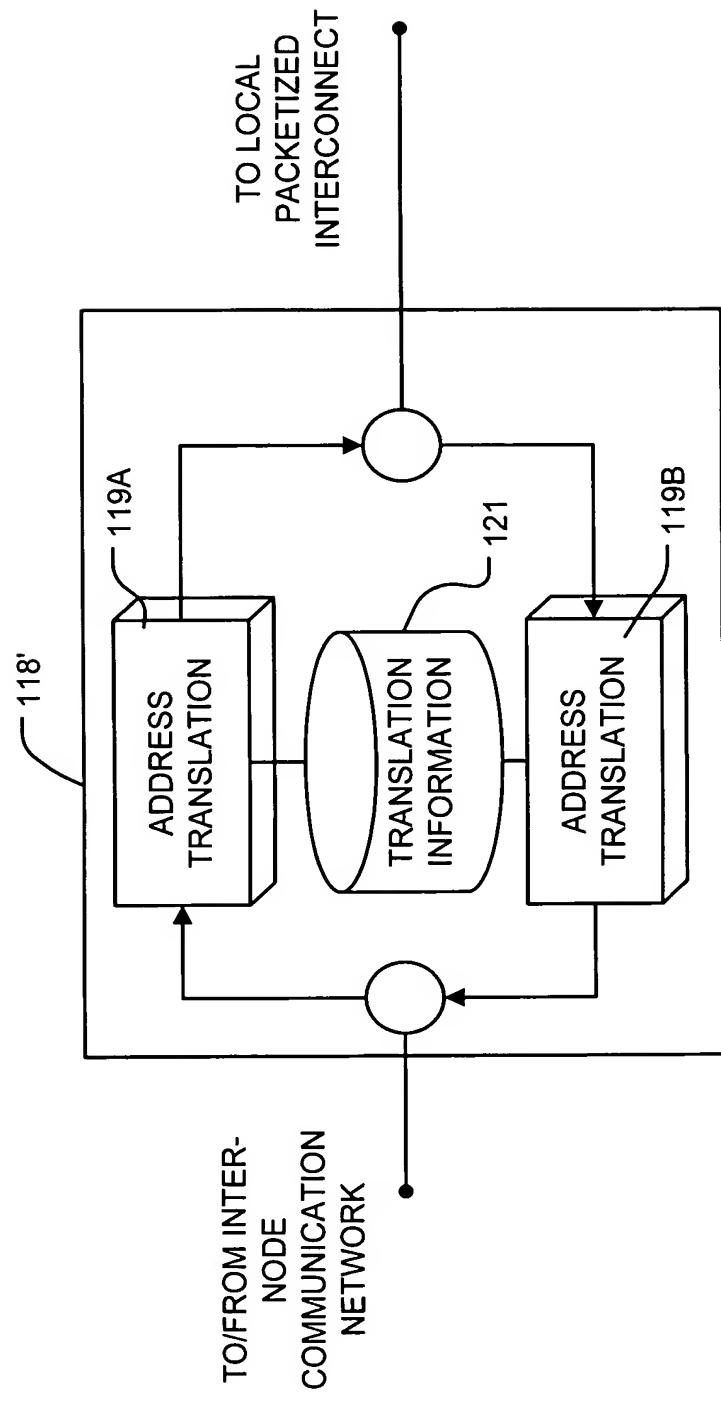


Figure 4A

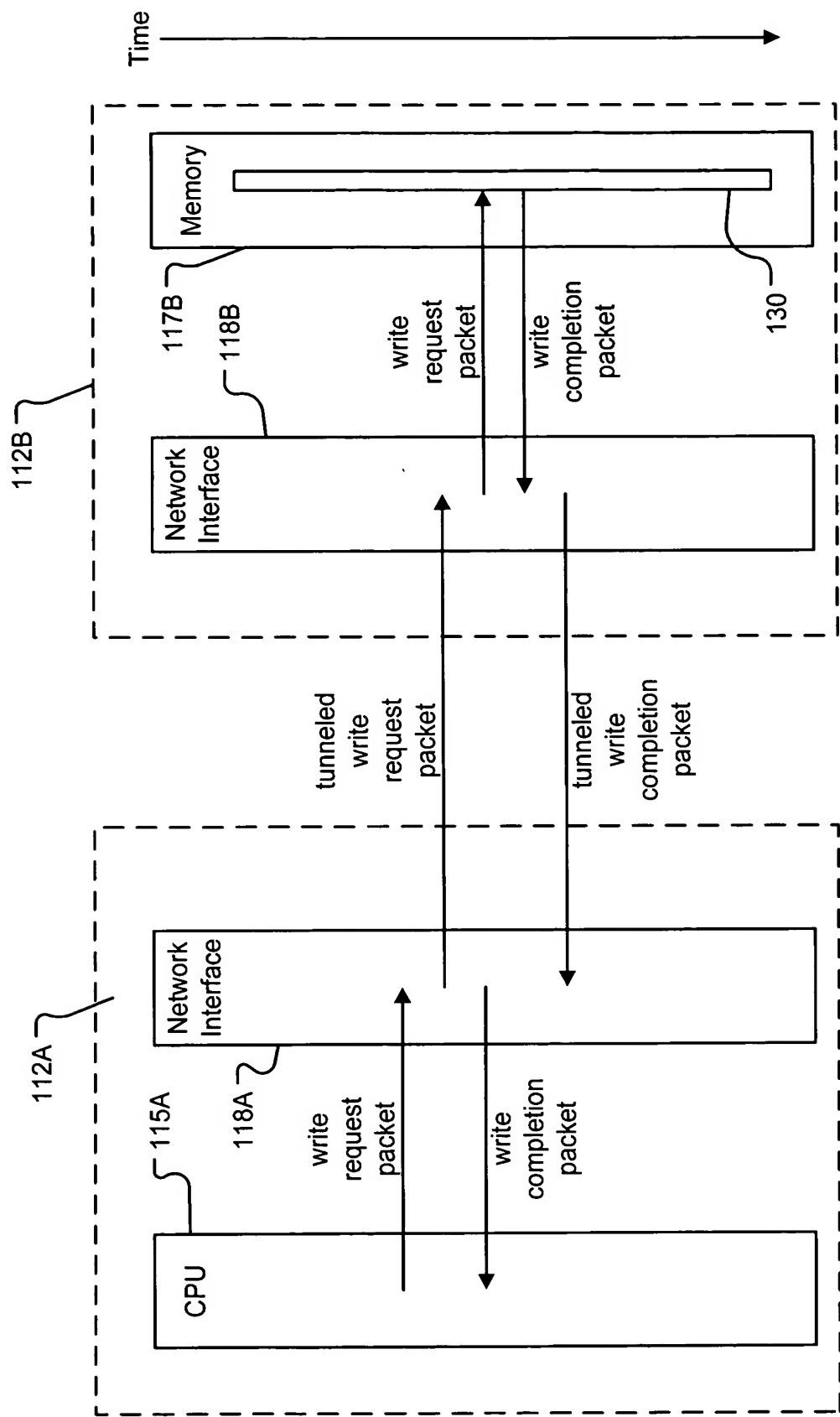


Figure 5

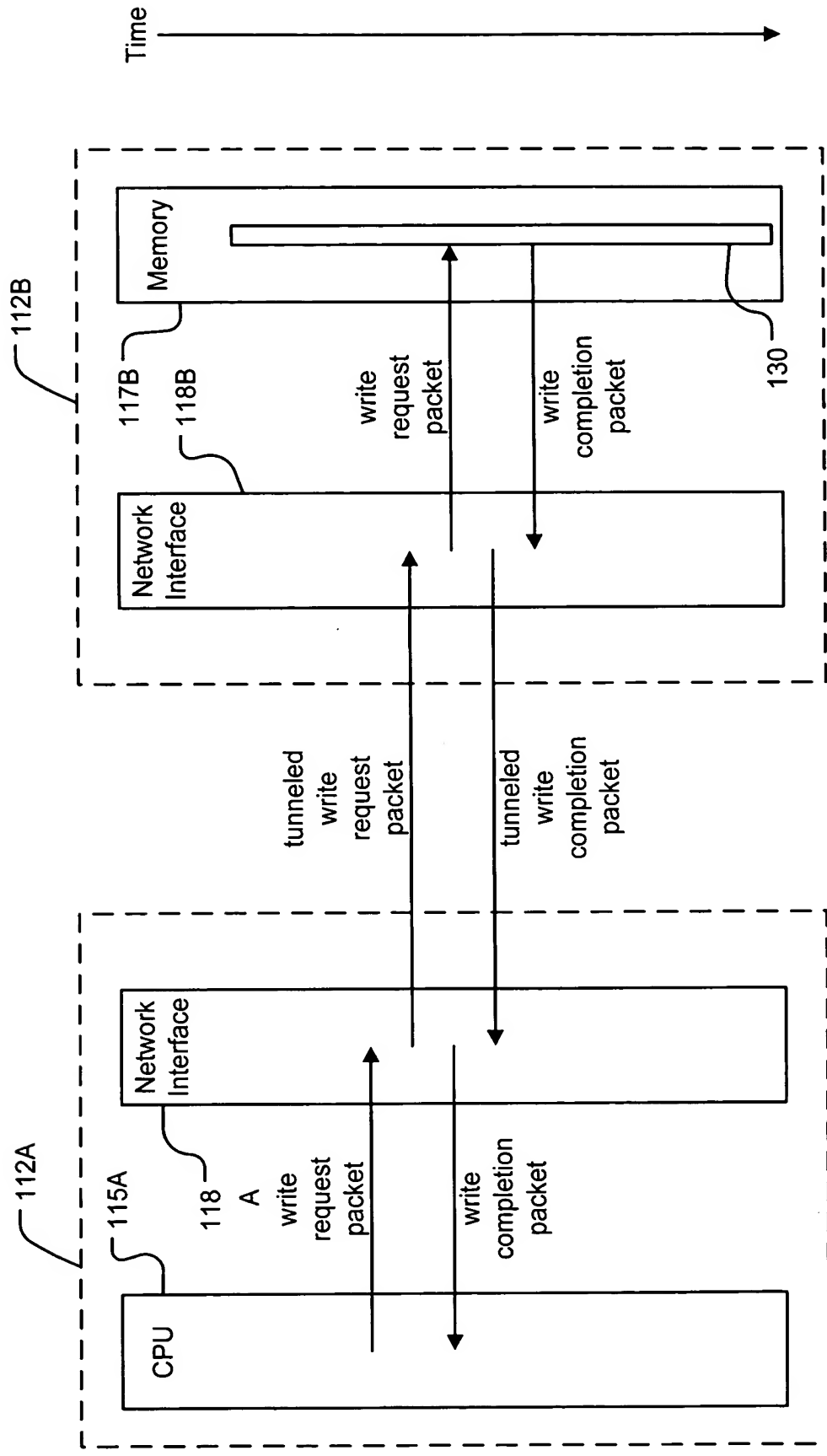


Figure 6

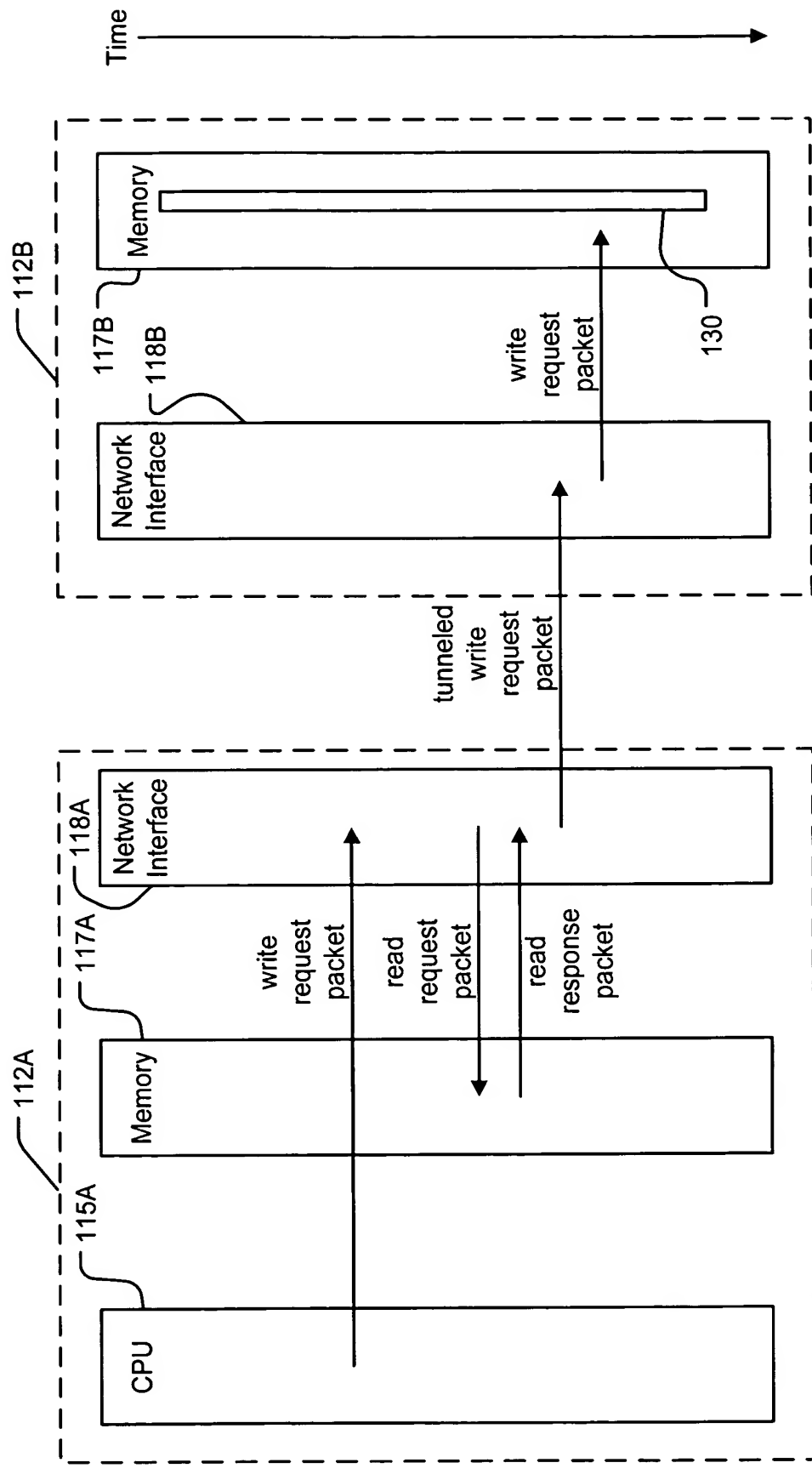


Figure 7

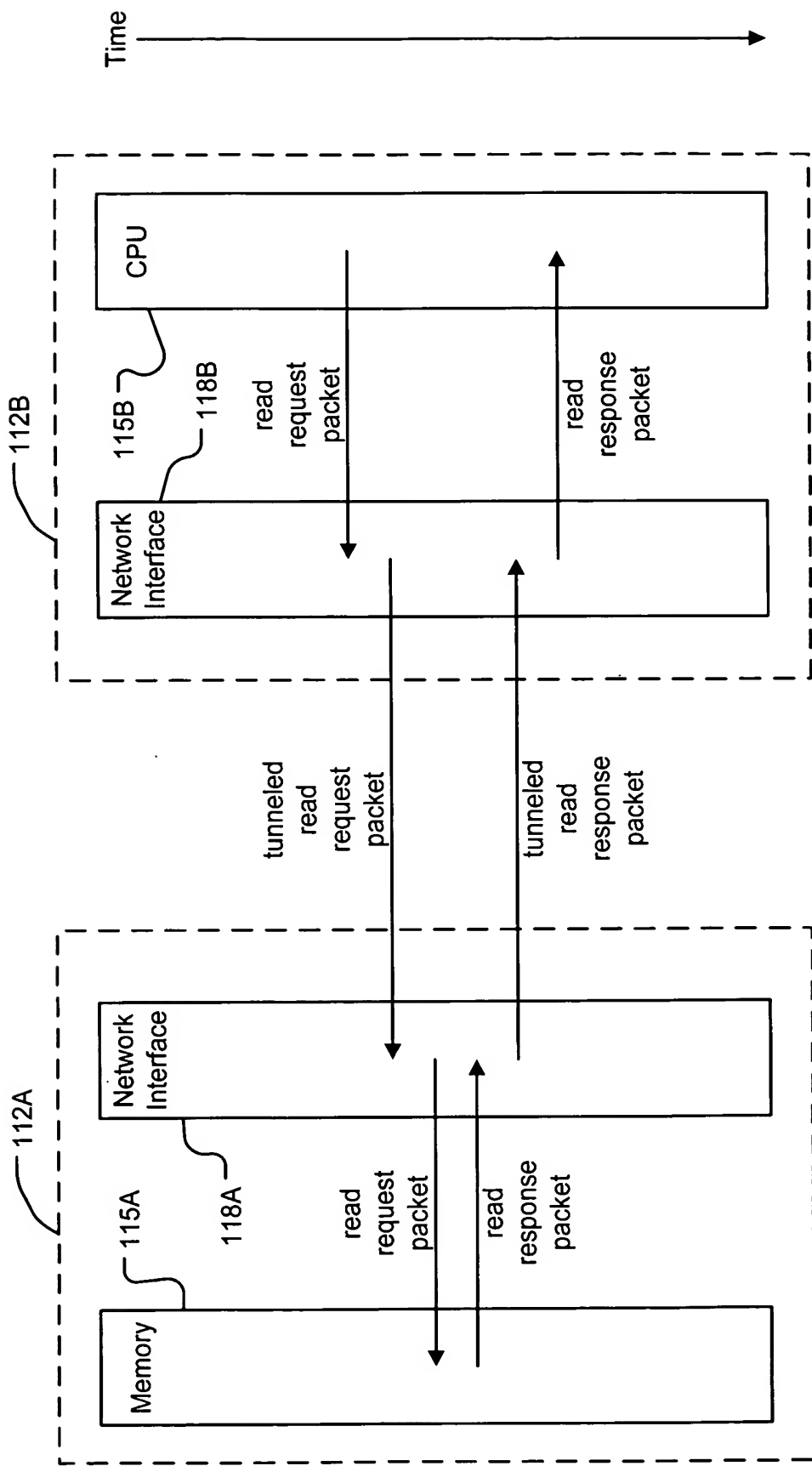
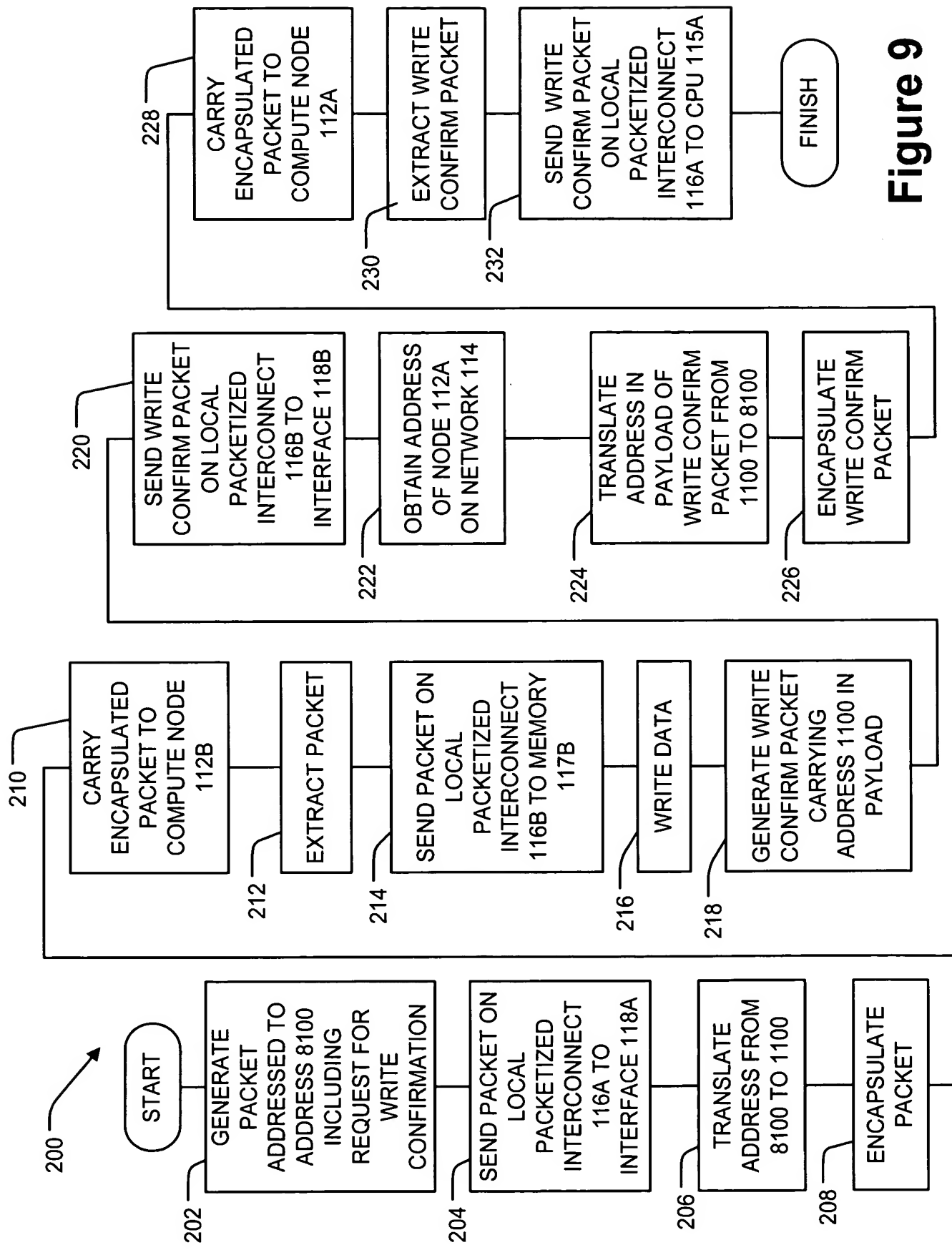


Figure 8



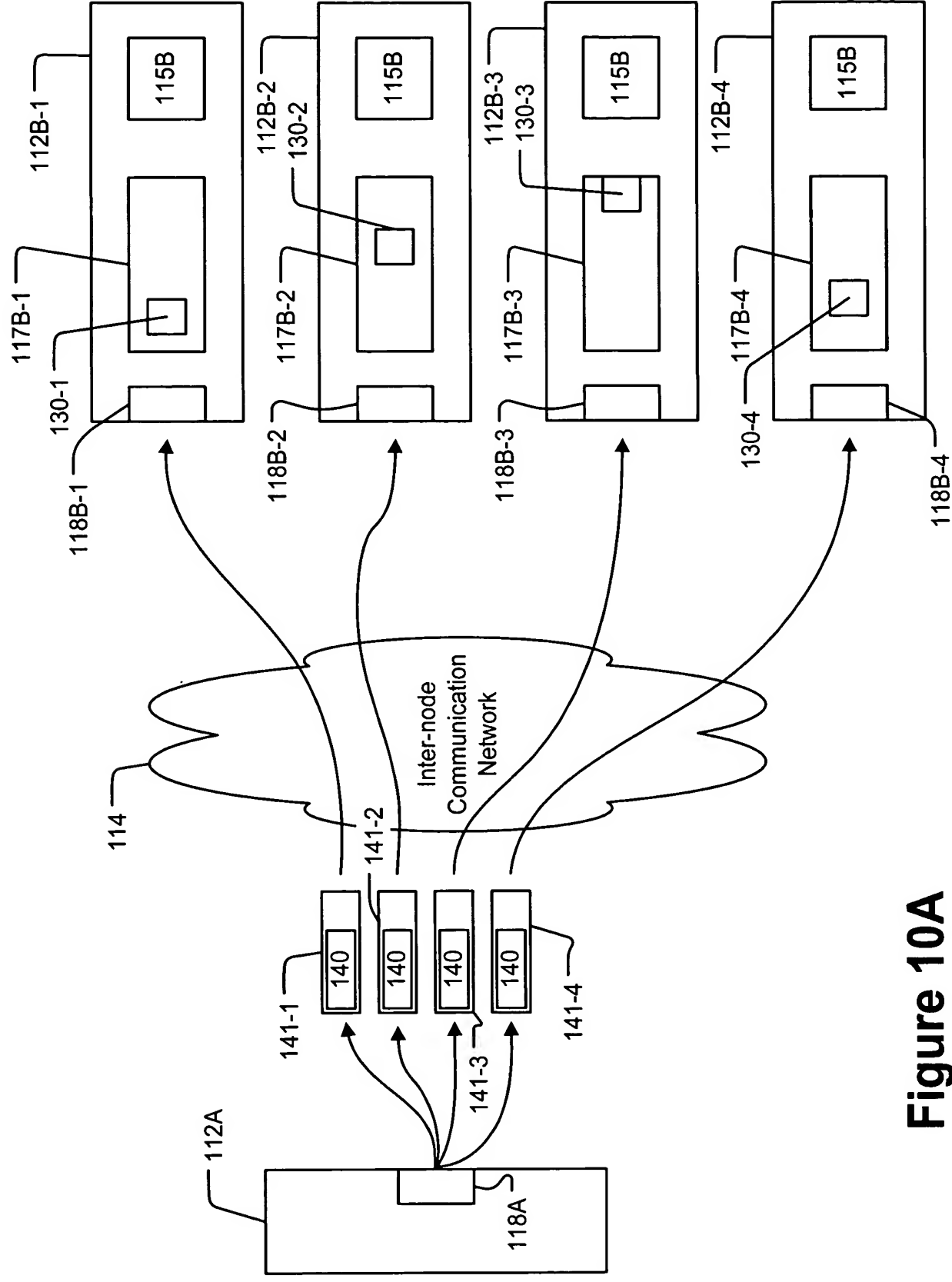


Figure 10A

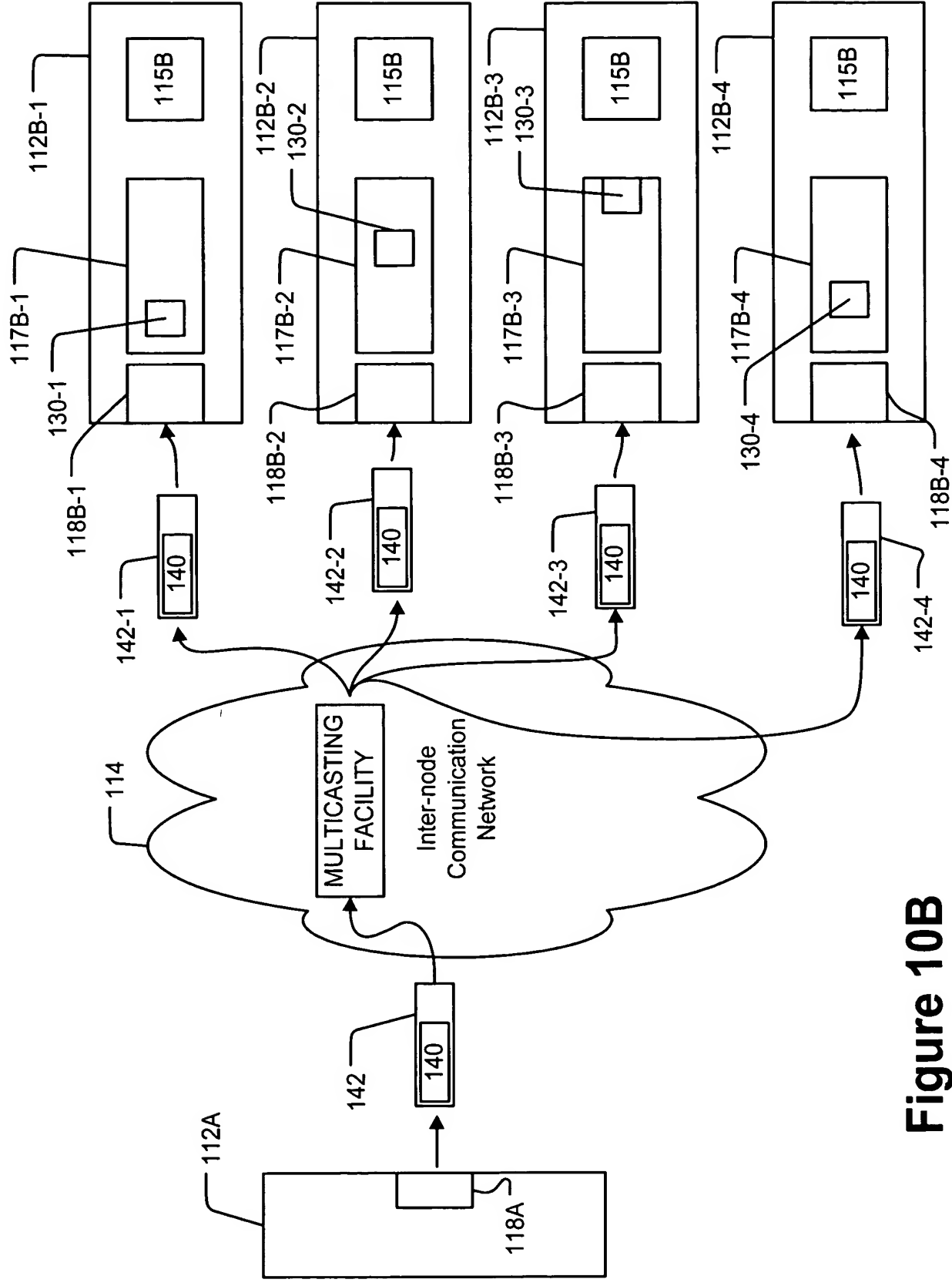


Figure 10B

ADDRESS SPACE
INTERFACE 118A CONTROL REGISTERS
MEMORY 117A
OTHER HARDWARE CONTROL REGISTERS
RANGE MAPPED TO INTERFACE 118A TO GO TO NODE 112B-1
RANGED MAPPED TO INTERFACE 118A TO GO TO FIRST LOCATIONS IN NODE 112B-3
RANGED MAPPED TO INTERFACE 118A TO GO TO SECOND LOCATIONS IN NODE 112B-3
RANGED MAPPED TO INTERFACE 118A TO GO TO LOCATIONS IN ALL OF NODES 112B-1, 112B-2, 112B-3 ... 112B-N
■ ■ ■
RANGE MAPPED TO INTERFACE 118A TO GO TO NODE 112B-N
CPU 115A

Figure 11